EXPEDITED PROCEDURE
Examining Group Number 2826

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Michael Bauer et al.	Examiner: Ahmed N. Sefer
Serial No.:	10/789,033	Group Art Unit: 2826
Filed:	February 27, 2004	Docket: I431.103.101/FIN 423 US
Title:	ELECTRONIC COMPONENT AND SEMICONDUCTOR WAFER, AND METHOD FOR PRODUCING THE SAME	

DECLARATION OF PRIOR INVENTION UNDER 37 C.F.R. § 1.131

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Declaration is submitted to establish prior invention of the subject matter of the present patent application. The person making this Declaration is one of the patent attorneys assigned to handle the patent application, Dr. Horst Schäfer. I am with the firm Schweiger and Partner, European Patent Attorneys.

Accompanying this is Invention Disclosure 2002E16516DE; and Translation of Invention Disclosure, which collectively establish conception of the subject matter of the present patent application prior to the effective reference date of January 16, 2003 of Yamaguchi U.S. Patent Publication 2004/0157410 and due diligence from prior to the effective reference date to the filing date of February 27, 2003 of the priory German Patent application (i.e., constructive reduction to practice), on which the present U.S. patent application is based.

Invention Disclosure 2002E16516DE was drafted by the inventors in German. This invention disclosure describes the subject matter of the present patent application. I translated Invention Disclosure 2002E16516DE from German into English.

Invention Disclosure 2002E16516DE was prepared on August 6, 2002 and was received by a representative of the employer on August 14, 2002. It was then transferred to the Siemens IP Department on October 1, 2002. It was given to Schweiger and Partner on 10.10.2002 with instructions to file a German patent application. An application was then promptly prepared with

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assistance from the inventors, reviewed and eventually signed by the inventors, and then filed in Germany on February 27, 2003.

As such, due diligence was exercised from prior to the effective reference date of January 16, 2003 of Yamaguchi U.S. Patent Publication 2004/0157410 to the filing date of the Germany Patent applicaiton on February 27, 2003, on which the present U.S. patent application is based (i.e., constructive reduction to practice).

As a person signing below, I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name: Dr. Horst Schäfer

Date: Dec. 13, 2005

Docket No. I431.103.101/FIN 423 US
Invention Disclosure 2002E16516DE (Translated)

Your ref. I431.103.101
Our ref. FIN 423 US

Translation of Invention disclosure

1. Which technical problem is to be solved by your invention?

The invention solves the problem of contacting/electrical connection between chip and the users circuit board (PCB) or module circuit board. We depart from the usual solution (intermediate step via packaging) and connect the chip directly with the PCB.

2. How has the problem been previously solved?

The electrical connection was previously realised either via the intermediate step of the packaging (QFP, BGA, QFN,...) or through wirebonding on board or flip-chip on board. The two last solutions are characterised in that the contact areas or bumps come to lie on the active chip surface.

3. How does your invention solve the given problem (give advantages)?

The invention is based on the basic principle of relocating the contacts to the four side edges of the chip. These contacts (castellations) can be produced in the wafer composite, for example in the following way (see picture 1): etching the contact holes, plating the contact holes, possibly filling up the contact holes with solder material, singulating the wafer.

The filling up of the contact holes with solder can be effected in different ways. Either through screen printing

(soldered paste is spread over the wafer into the contact holes and afterwards remelted)or also through squeezing preformed solder balls into the contact holes (and finally remelting the solder).

After the singulation of the wafer (the saw path central through the contact holes), the chip is ready for respective further processing (with or without solder deposits in the contacts) - see picture 2.

This chip can now be contacted to the PCB in different ways: in a contact socket with corresponding side contacts (see picture 3), soldering the chip in the lateral plane on contact pads with or without solder (see picture 4), as picture 4 however in combination with WB (Wire bonds) and possibly with full area rear side soldering (see figure 5), soldering the chip in a perpendicular plane (see picture 6) or in the application for stacked chips (see picture 7).

The mechanical and/or protection from environmental influences can on the one hand be effected by mounting the chip with the active side downwards and additionally through the deposition of a protective coating on the PCB.

4. Where does the inventive step lie?

The inventive step lies in the use of perpendicular contact holes on silicon chips. Thereby, one can achieve the following advantages over usual packages:

- Avoidance of additional packaging materials
- Since no additional materials are used, also no MSL problems
- Avoidance of parasitic contact paths
- Direct processing with standard SMT processes possible

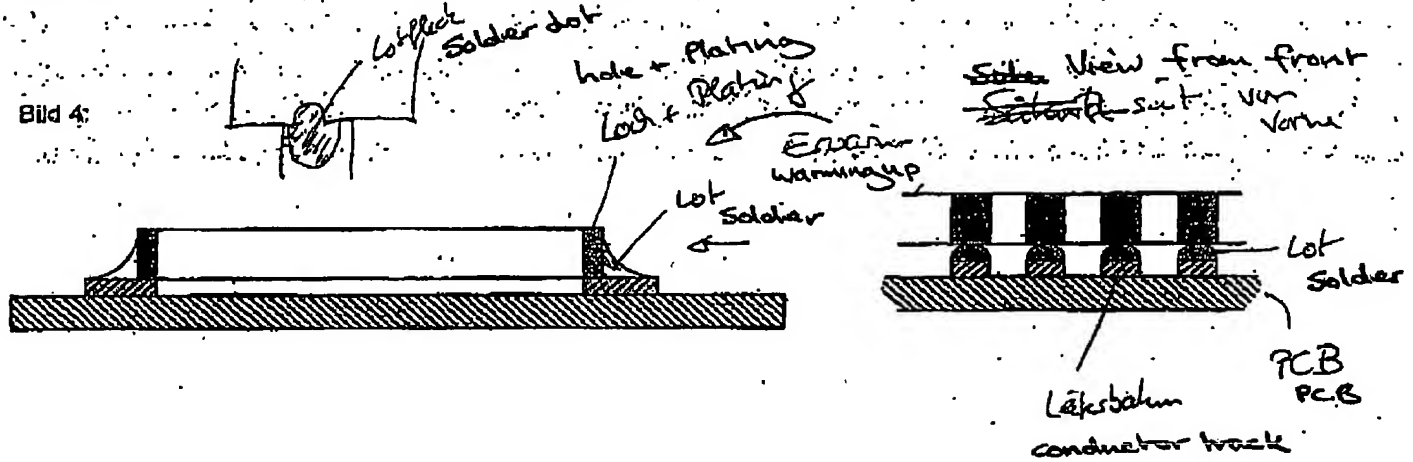
- Direct combination of wire bonds and solder balls possible
- Perpendicular contacting of chips possible (memory, LEDs,...)
- Simple stackability of chips (memory, ...)

5. Embodiments of the invention.

6. For further explanation as annexes are attached:
- sheet of the depiction of one or more embodiments of the invention:
  (if possible, prepare drawings in PowerPoint or designer format)
- sheet of additional descriptions (for example laboratory reports, experiment logs);
- sheet literature, which describes the prior art from which the invention emanates; *
- other documents (for example discs, particularly with drawings of the embodiments):

* please photocopy or print especially all cited publications (Essays completely; by books the relevant chapter) with complete bibliographic data attached.

Bild 4:



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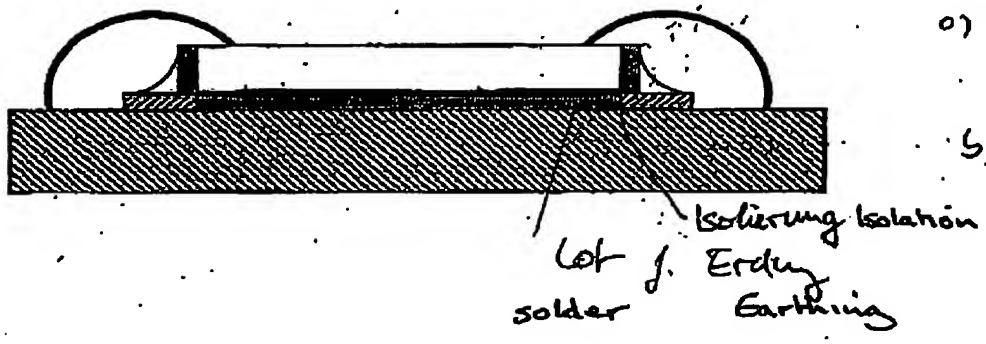

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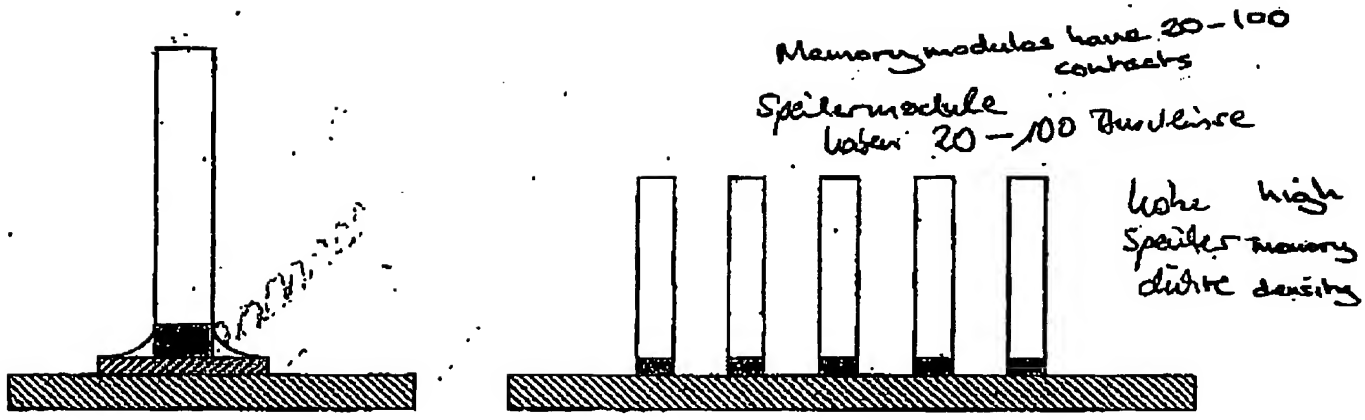

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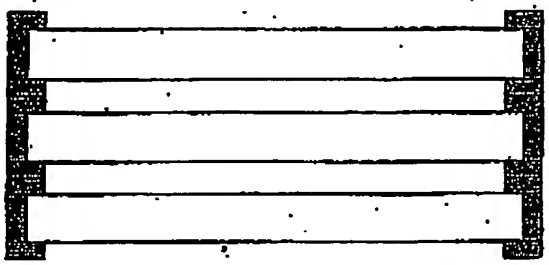

Stapeln
bei Speicherzelle
1-2 Ausgänge
sind mit
miteinander verbunden

Stacking
by memory position
1-2 contacts
are connected
with each other

6. Zur weiteren Erläuterung sind als Anlagen beigefügt:

_____ Blatt der Darstellung eines oder mehrerer Ausführungsbeispiele der Erfindung;
(falls möglich, Zeichnungen im PowerPoint- oder Designer-Format anfertigen)

_____ Blatt zusätzliche Beschreibungen (z.B. Laborberichte, Versuchsprotokolle);

_____ Blatt Literatur, die den Stand der Technik, von dem die Erfindung ausgeht, beschreibt; *)

_____ sonstige Unterlagen (z.B. Disketten, insbesondere mit Zeichnungen der Ausführungsbeispiele):

*) Bitte Fotokopien oder Sonderdrucke aller zitierten Veröffentlichungen (Aufsätze vollständig, bei Büchern die relevanten Kapitel) mit vollständigen bibliographischen Daten beifügen.